

WHAT IS CLAIMED IS:

- 1           1.    A    method    for    supporting    software    pipelining,  
2    comprising:  
3                receiving a shift mask signal;  
4                receiving a shift signal;  
5                identifying a shifting register queue based on the  
6    shift mask signal, the shifting register queue comprising a  
7    plurality of queue registers; and  
8                shifting the contents of the queue registers based on  
9    the shift signal.
- 1           2.    The method of Claim 1, receiving the shift mask signal  
2    comprising receiving the shift mask signal from a shift mask  
3    register.
- 1           3.    The method of Claim 1, receiving the shift signal  
2    comprising receiving the shift signal from an external  
3    component.

1           4.    The method of Claim 1, the shifting register queue  
2   part of a register file, the register file comprising the  
3   plurality of queue registers and comprising a plurality of non-  
4   queue registers, the shift mask signal comprising a plurality of  
5   bits, each bit associated with a corresponding register in the  
6   register file.

1           5.    The method of Claim 4, the bits in the shift mask  
2   signal corresponding to the queue registers comprising 1s, and  
3   the bits in the shift mask signal corresponding to the non-queue  
4   registers comprising 0s.

1           6.    The method of Claim 4, the bits in the shift mask  
2   signal corresponding to the queue registers comprising 0s, and  
3   the bits in the shift mask signal corresponding to the non-queue  
4   registers comprising 1s.

1           7.    A    system   for   supporting   software   pipelining,  
2   comprising a register file comprising a plurality of registers,  
3   the registers comprising queue registers and non-queue  
4   registers, the queue registers forming a shifting register  
5   queue, at least one non-queue register located between two queue  
6   registers.

1           8.    The system of Claim 7, further comprising a shift mask  
2   register operable to identify the queue registers within the  
3   register file.

1           9.    The system of Claim 8, the shift mask register further  
2   operable to provide a shift mask signal to the register file,  
3   the shift mask signal operable to identify the queue registers  
4   for the register file.

1           10. The system of Claim 7, the register file further  
2 comprising write decoding logic and a plurality of multiplexers,  
3 the write decoding logic operable to generate control signals  
4 and write signals, each multiplexer corresponding to a register  
5 within the register file, each multiplexer operable to receive  
6 one of the control signals from the write decoding logic and to  
7 provide write data to the corresponding register based on the  
8 control signal.

1           11. The system of Claim 10, the registers within the  
2 register file comprising edge-triggered flip-flops, each  
3 register operable to receive the write data from the multiplexer  
4 and to receive one of the write signals from the write decoding  
5 logic.

1           12. The system of Claim 11, for each register other than a  
2 first register, the write data provided by each multiplexer to  
3 the corresponding register based on the control signal  
4 comprising data from a previous register in the register file.

1           13. A system for supporting software pipelining,  
2 comprising a register file comprising a plurality of registers,  
3 the register file operable to receive a shift mask signal and a  
4 shift signal, to identify a shifting register queue within the  
5 register file based on the shift mask signal, the shifting  
6 register queue comprising a plurality of queue registers, and to  
7 shift the contents of the queue registers based on the shift  
8 signal.

1           14. The system of Claim 13, further comprising a shift  
2 mask register operable to identify the queue registers within  
3 the register file.

1           15. The system of Claim 14, the shift mask register  
2 further operable to provide the shift mask signal to the  
3 register file.

1           16. The system of Claim 13, the shift mask signal  
2 comprising a plurality of bits, each bit associated with a  
3 corresponding register in the register file.

1           17. The system of Claim 13, the register file further  
2 comprising write decoding logic and a plurality of multiplexers,  
3 the write decoding logic operable to generate control signals  
4 and write signals, each multiplexer corresponding to a register  
5 within the register file, each multiplexer operable to receive  
6 one of the control signals from the write decoding logic and to  
7 provide write data to the corresponding register based on the  
8 control signal.

1           18. The system of Claim 17, the registers within the  
2 register file comprising edge-triggered flip-flops, each  
3 register operable to receive the write data from the multiplexer  
4 and to receive one of the write signals from the write decoding  
5 logic.

1           19. The system of Claim 18, for each register other than a  
2 first register, the write data provided by each multiplexer to  
3 the corresponding register based on the control signal  
4 comprising data from a previous register in the register file.

1           20. The system of Claim 13, the register file operable to  
2 receive the shift signal from an external component.